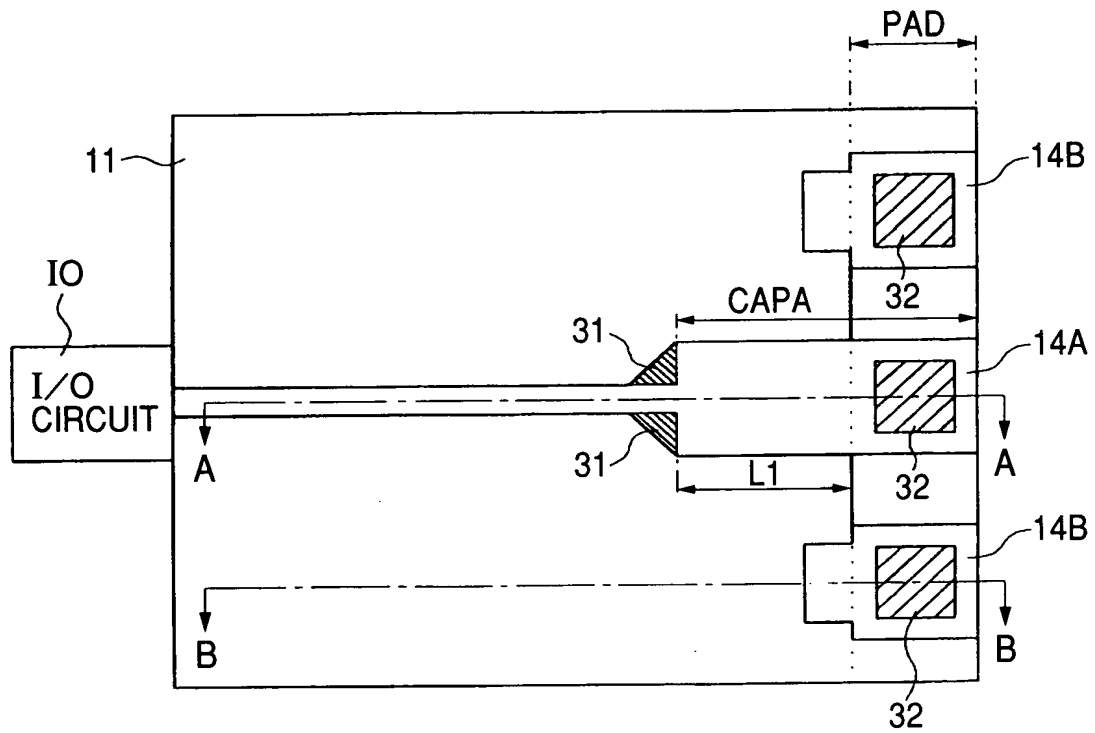
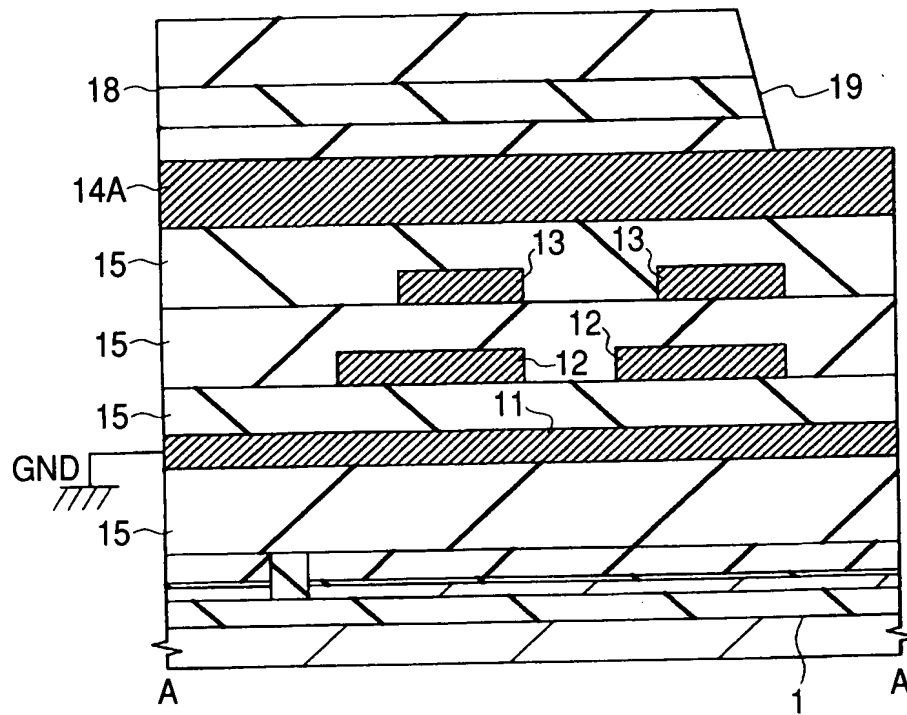


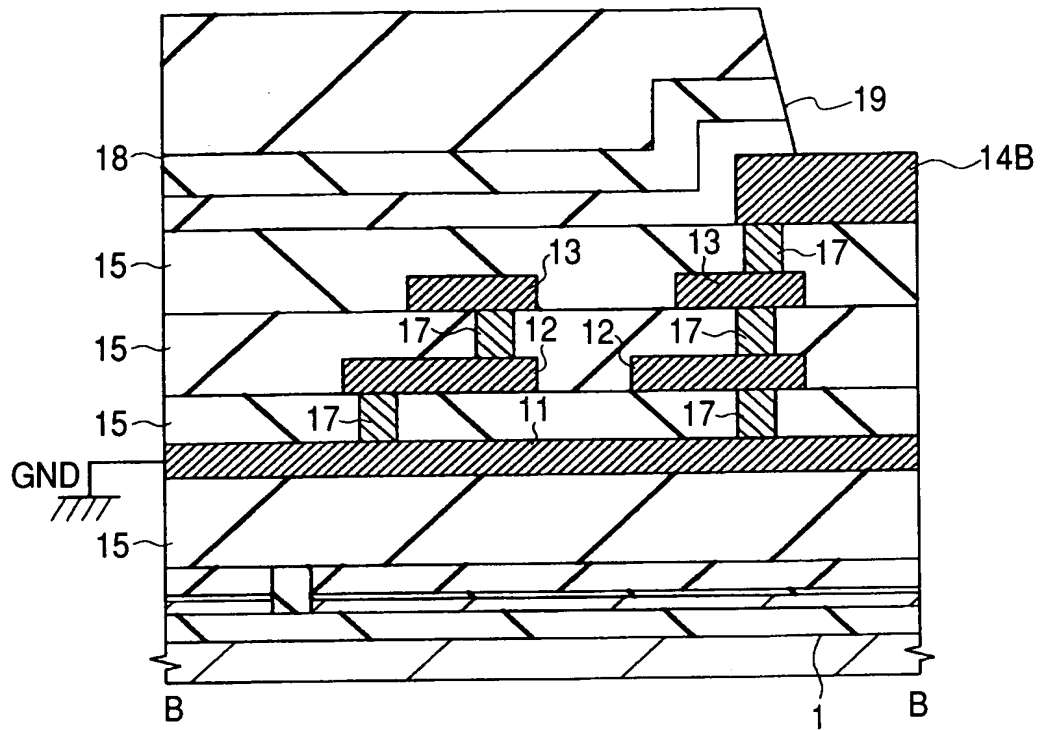
**FIG. 1**

11 : FIRST-LAYER WIRING (FIRST WIRING)  
 14A : FOURTH-LAYER WIRING (FOURTH WIRING)

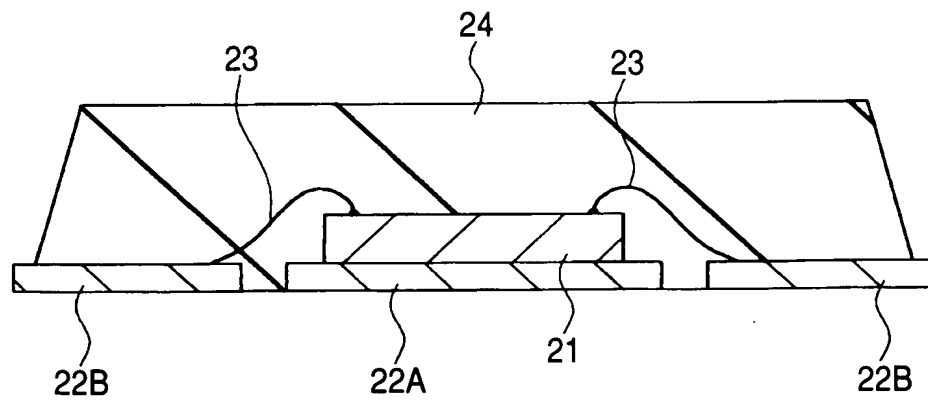
FIG. 2

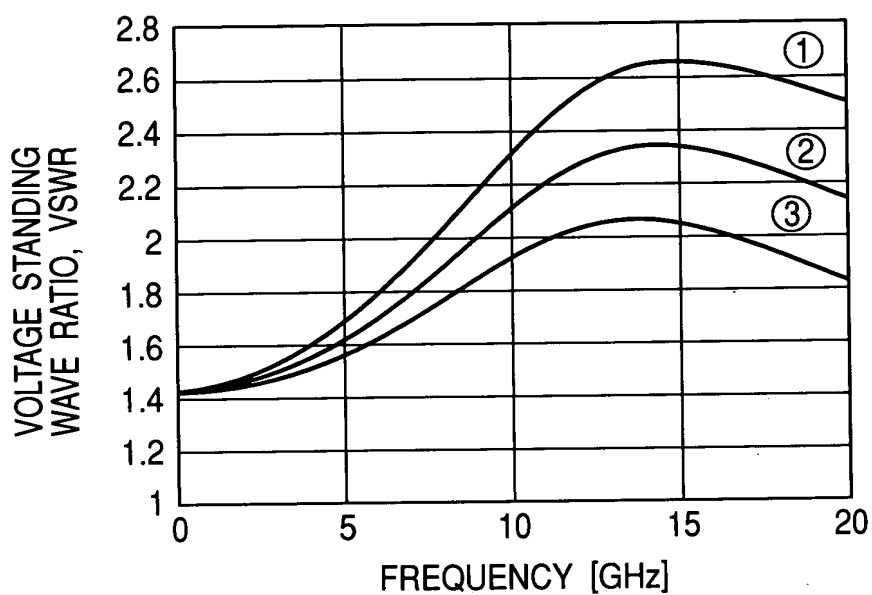


**FIG. 3**



**FIG. 4**

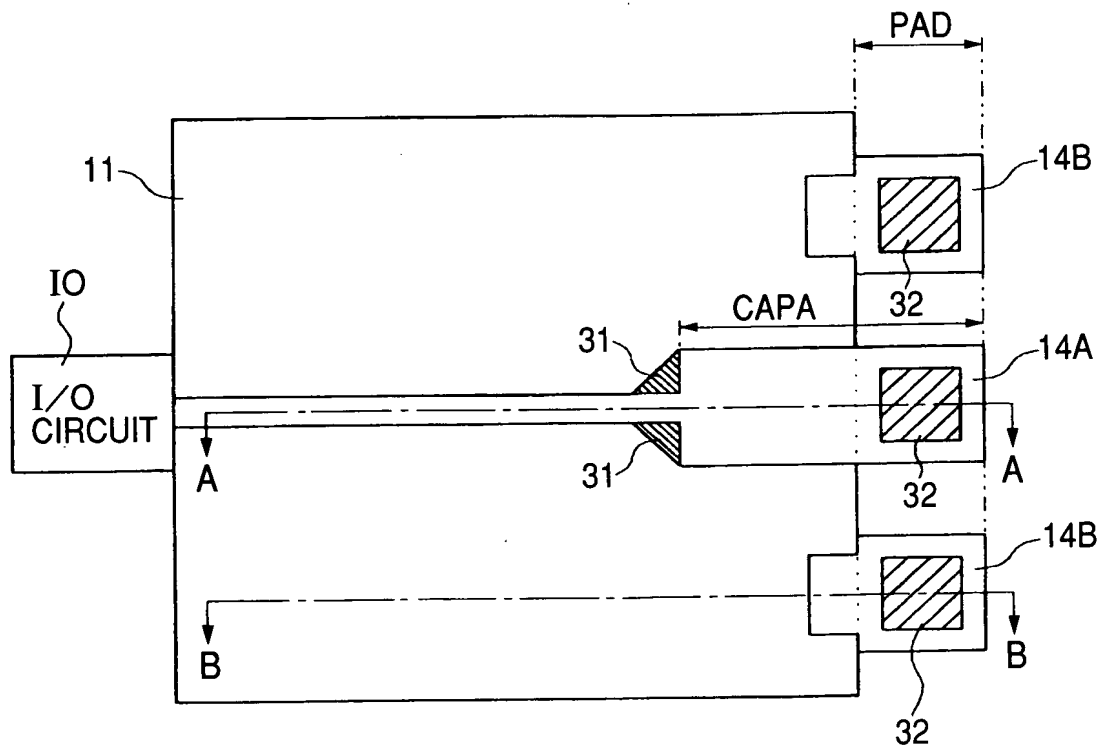


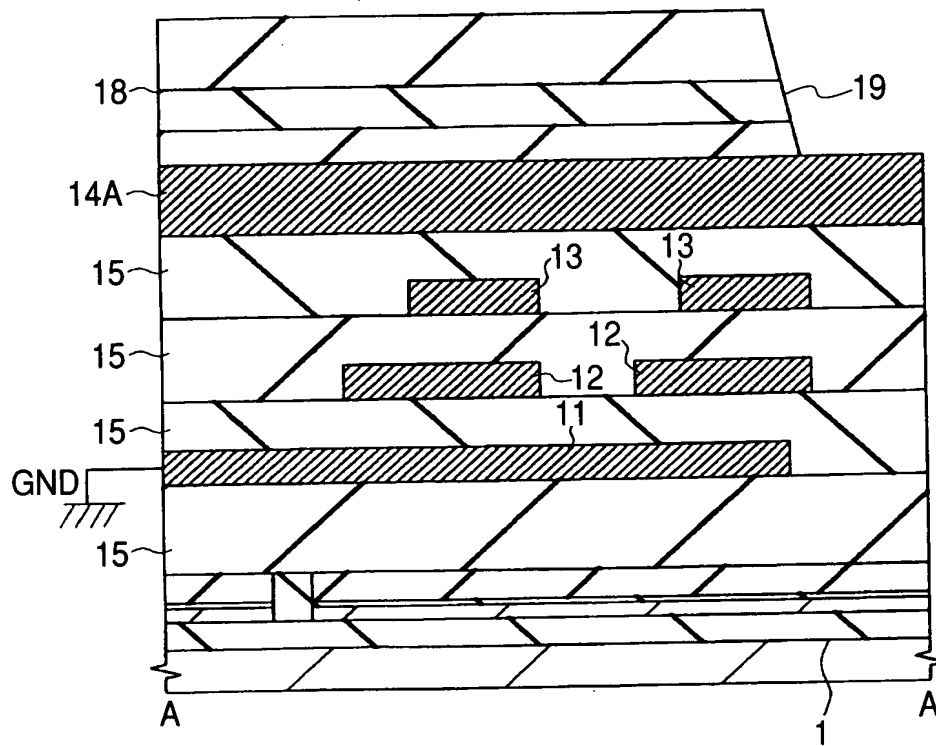
**FIG. 5**

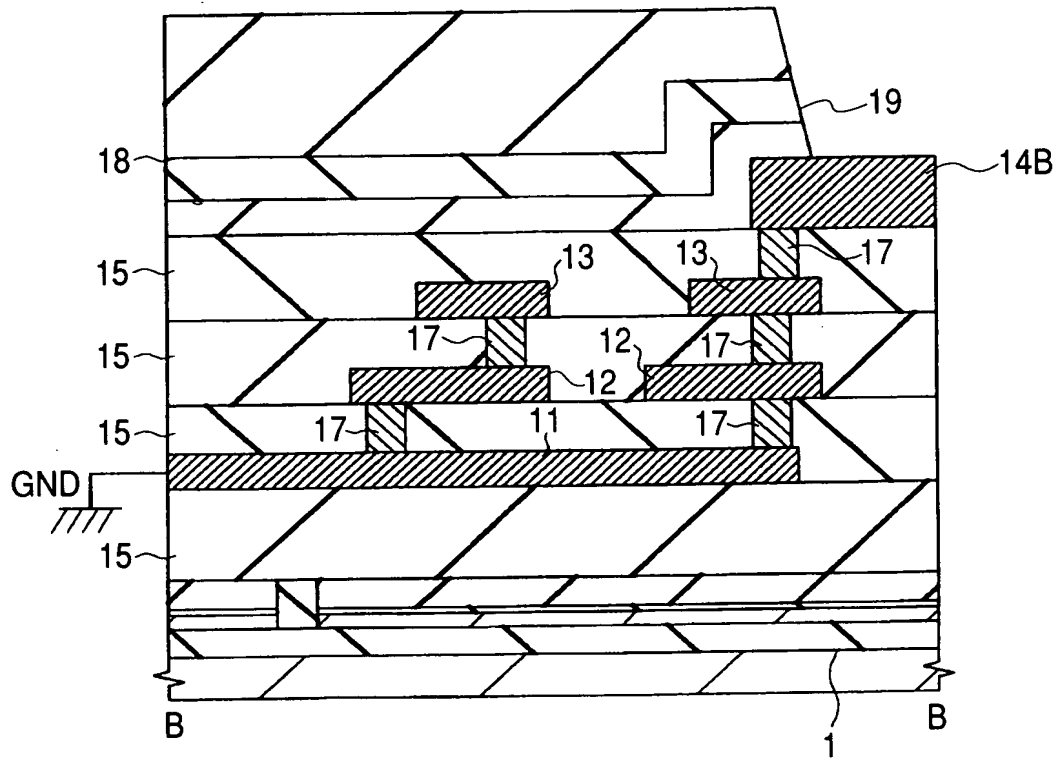
WIRE INDUCTANCE : 1nH

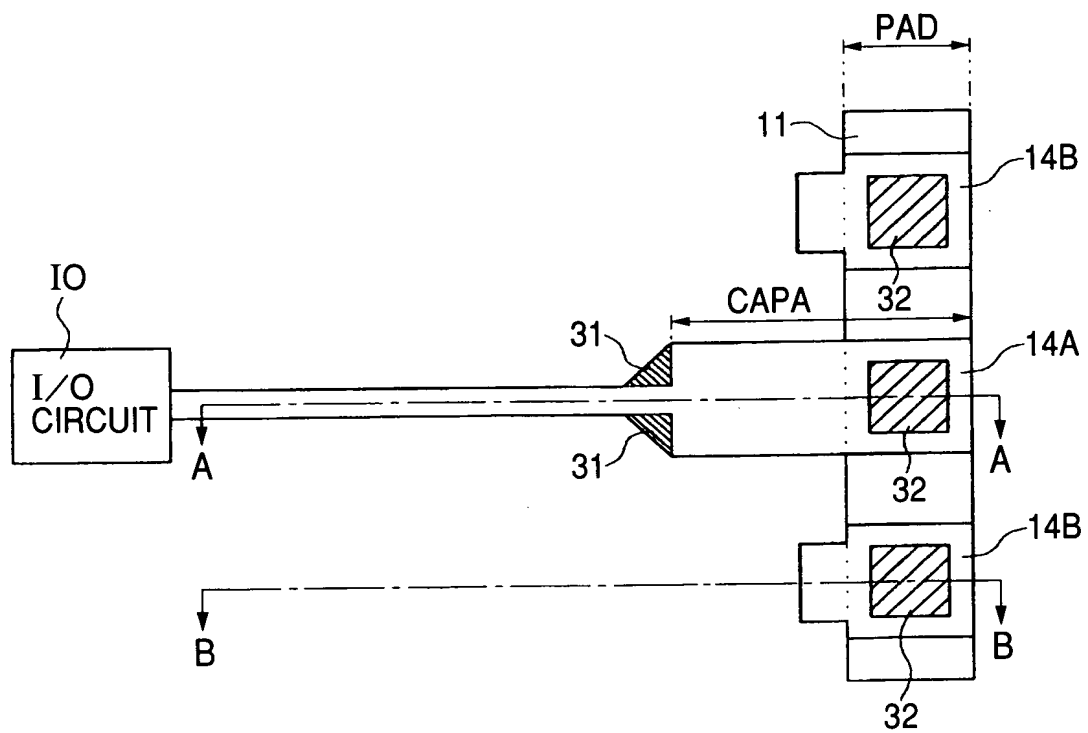
No.	L	VSWR ( $\leq 12\text{GHz}$ )	TRANSMISSION LOSS ( $\leq 12\text{GHz}$ )	DECISION	REASON
①	$0\ \mu\text{m}$	2.7	-0.1dB	×	LARGE VSWR
②	$50\ \mu\text{m}$	2.4	-0.3dB	○	MOST SUITABLE
③	$100\ \mu\text{m}$	2.1	-0.5dB	×	LARGE LOSS

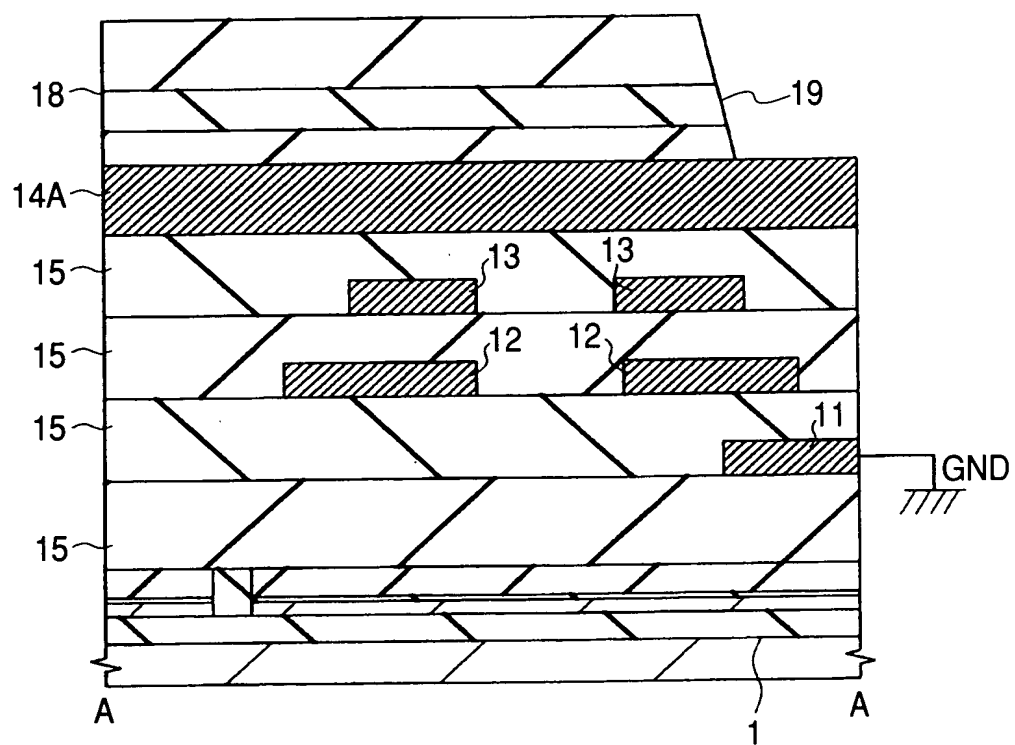
**FIG. 6**

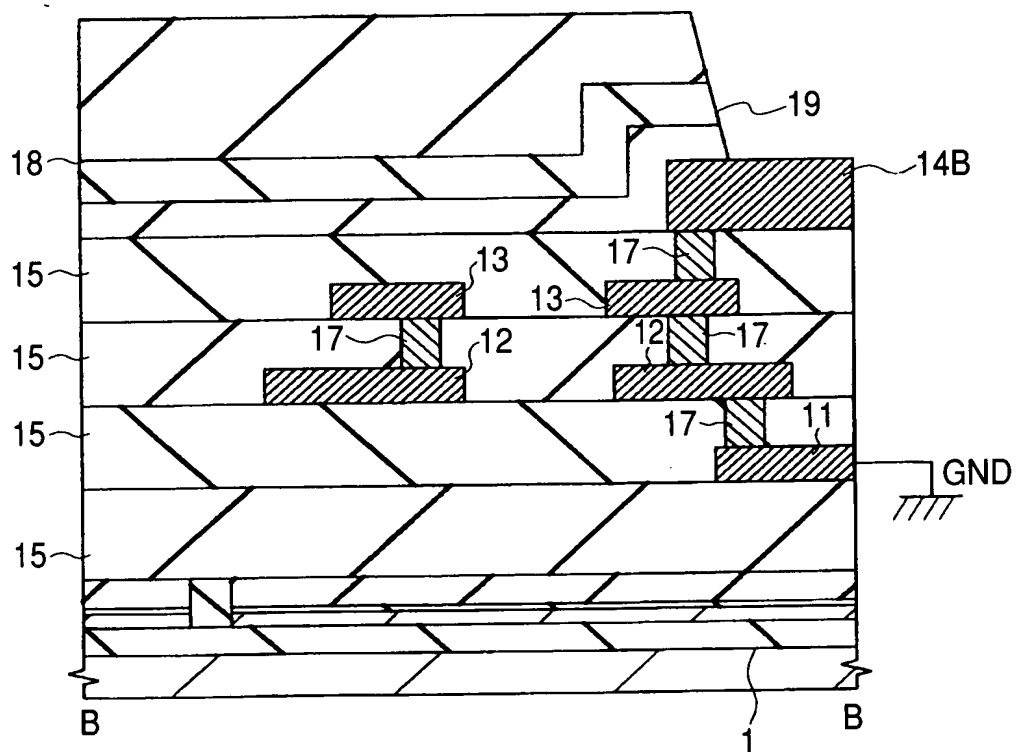


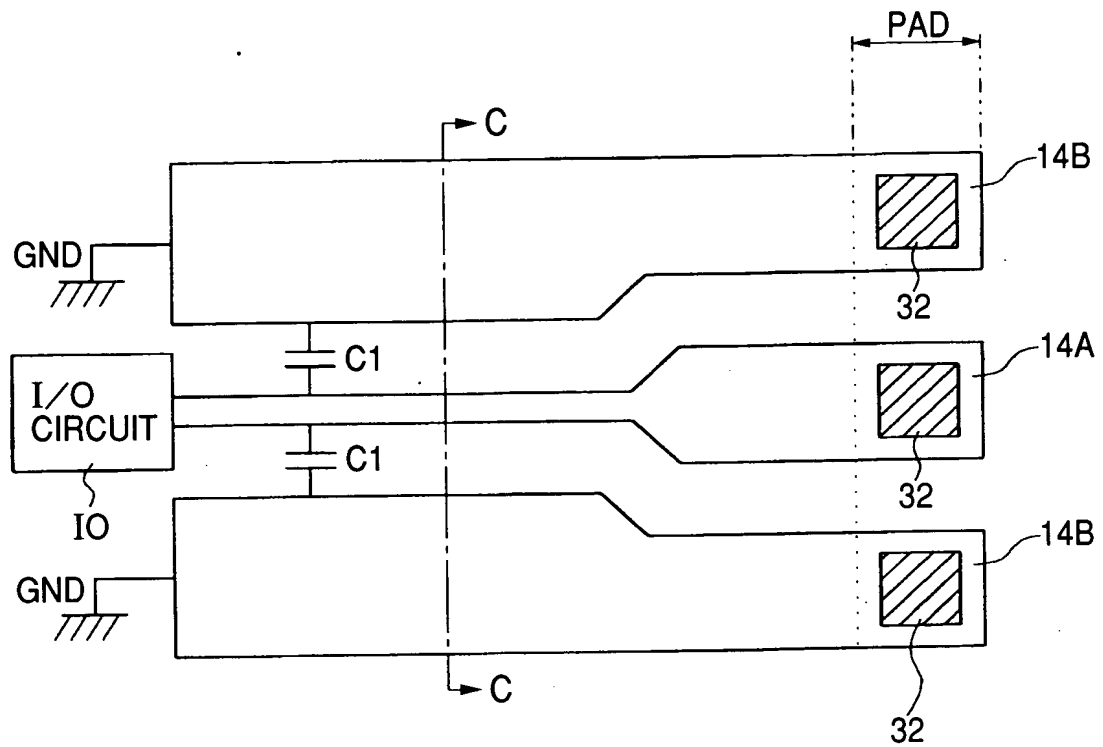
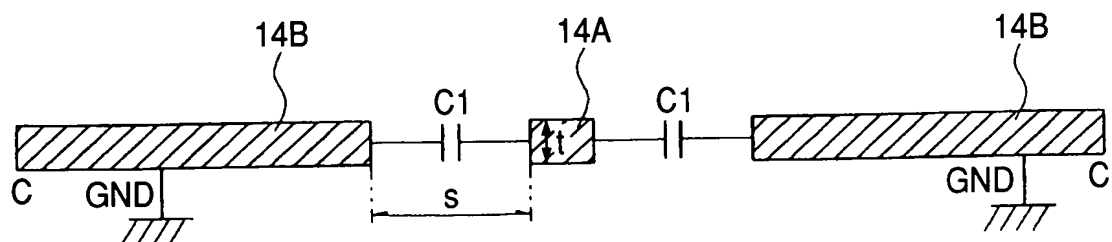
**FIG. 7**

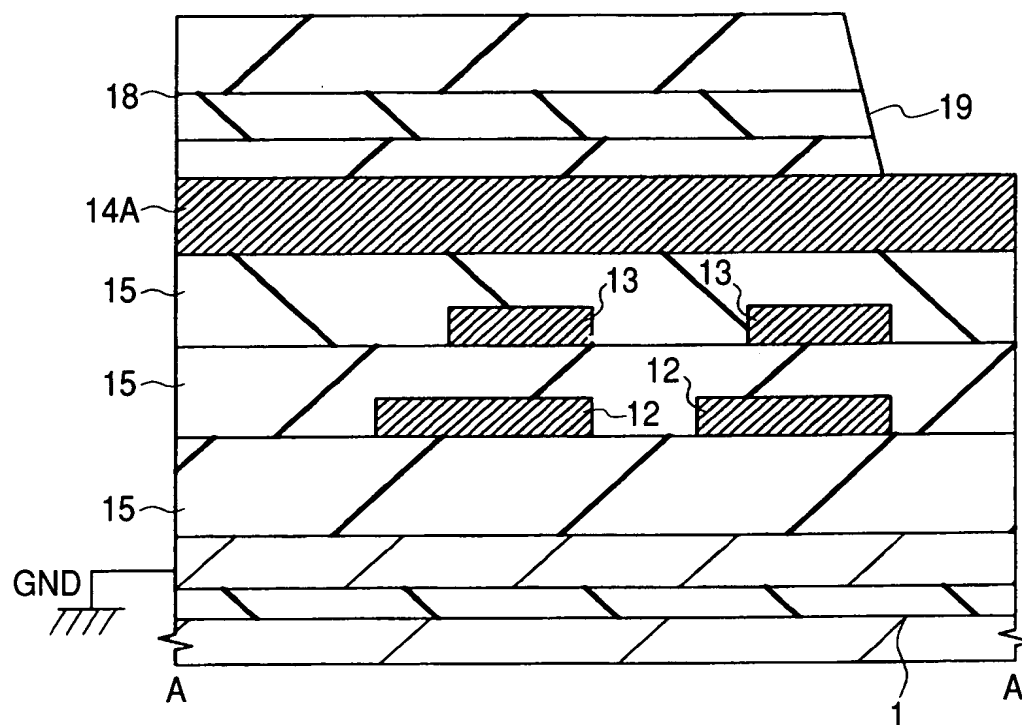
**FIG. 8**

**FIG. 9**

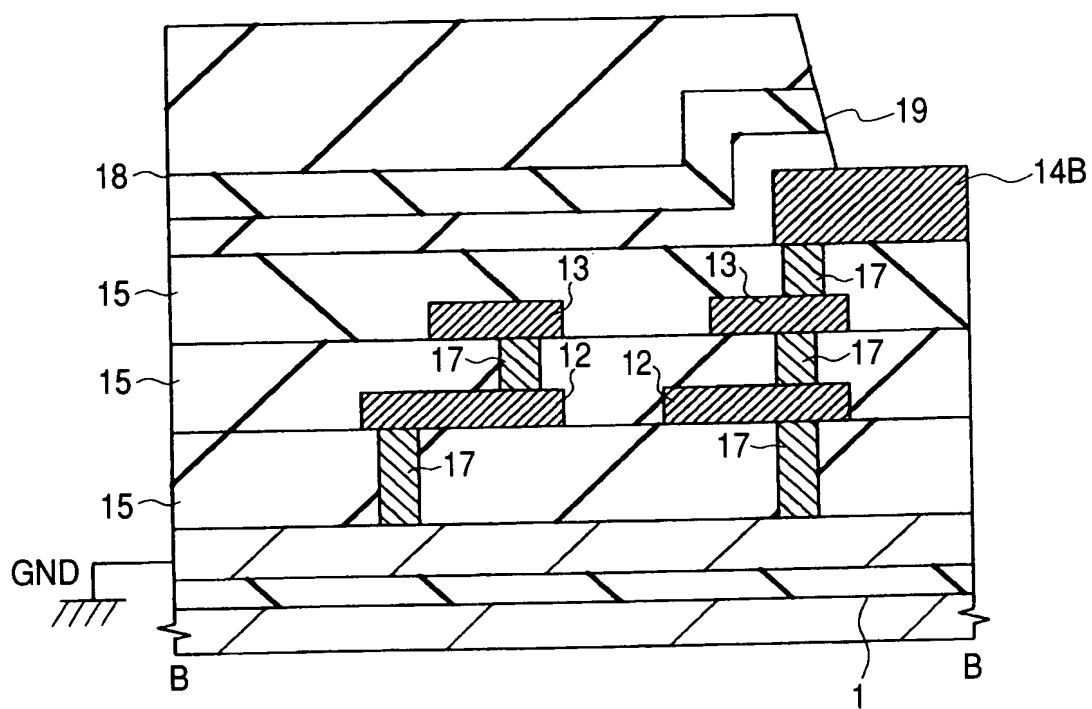
*FIG. 10*

**FIG. 11**

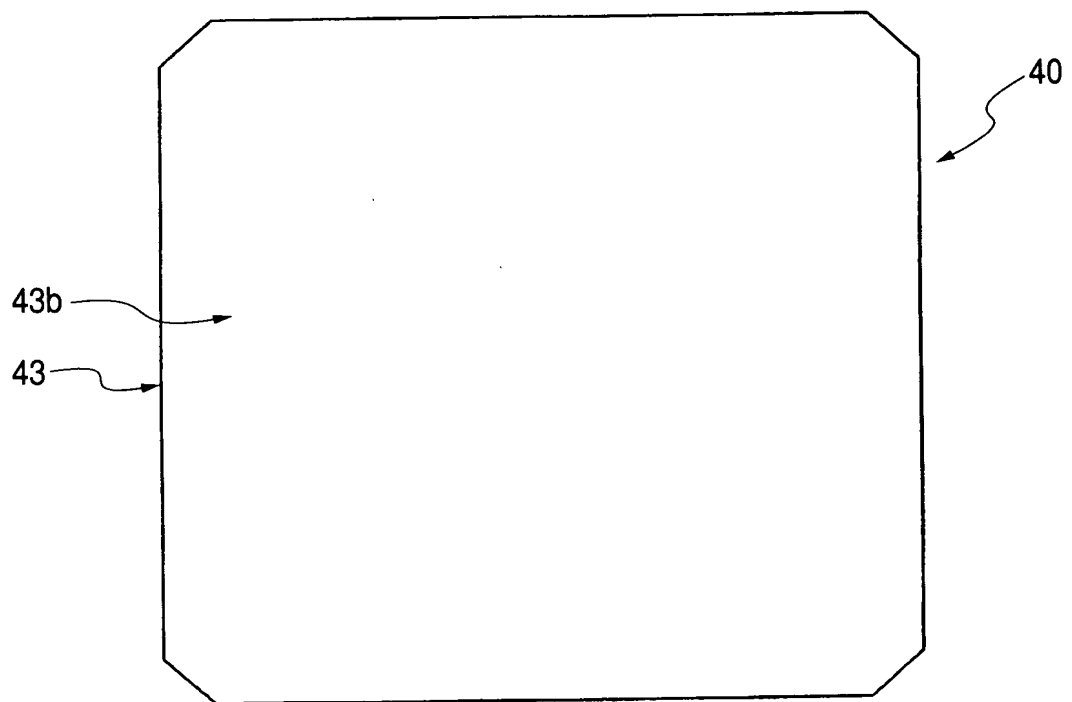
**FIG. 12****FIG. 13**

*FIG. 14*

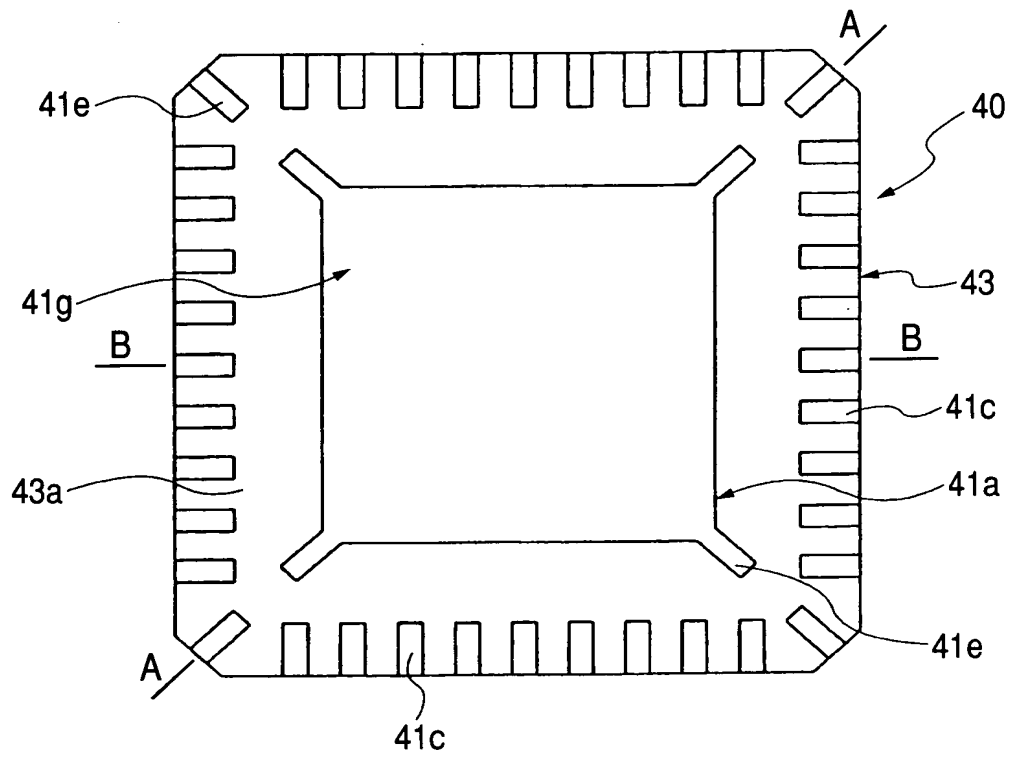
**FIG. 15**



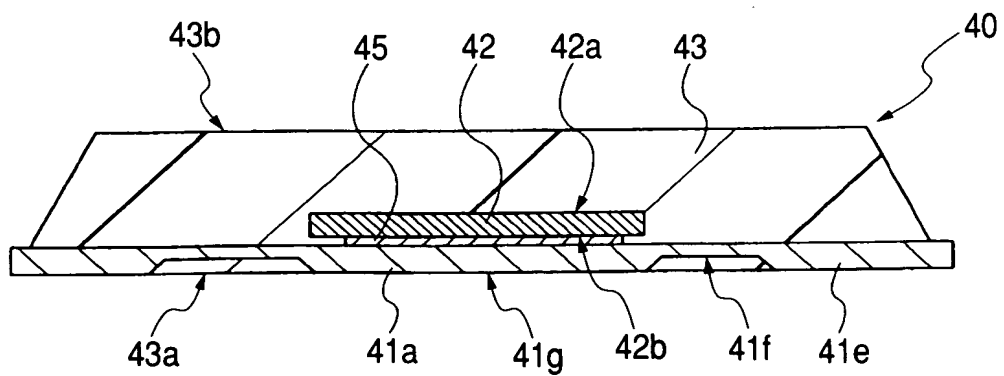
*FIG. 16*

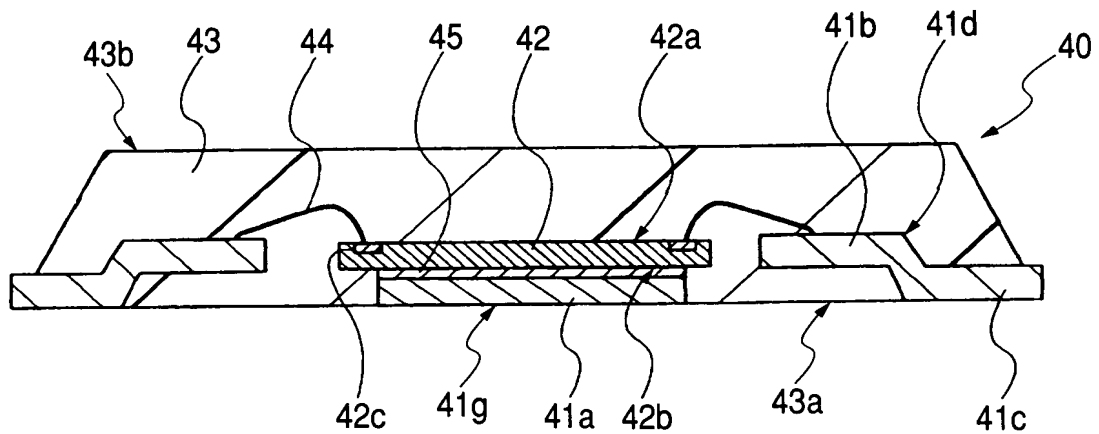


**FIG. 17**



**FIG. 18**



**FIG. 19**

- 40 : QFN (SEMICONDUCTOR DEVICE)
- 41a : DIE PAD
- 41b : INNER LEAD PORTION
- 41c : OUTER TERMINAL PORTION
- 41d : LEAD
- 42 : SEMICONDUCTOR CHIP
- 42a : MAIN SURFACE
- 42b : BACK SURFACE
- 42c : BONDING PAD (ELECTRODE)
- 43 : SEALING MEMBER
- 43a : MOUNTING SURFACE
- 43b : SURFACE (OPPOSITE SIDE)
- 44 : BONDING WIRE

FIG. 20

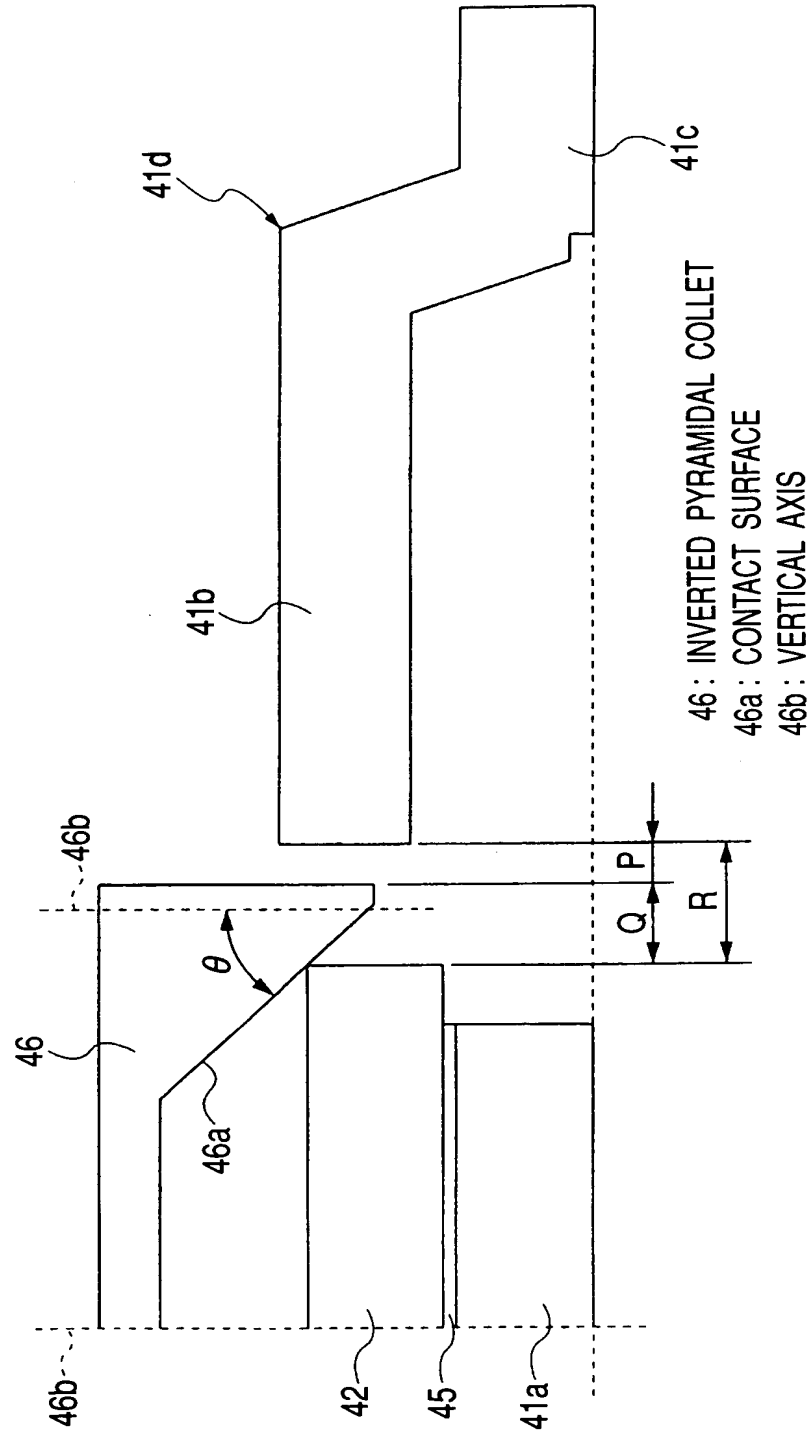
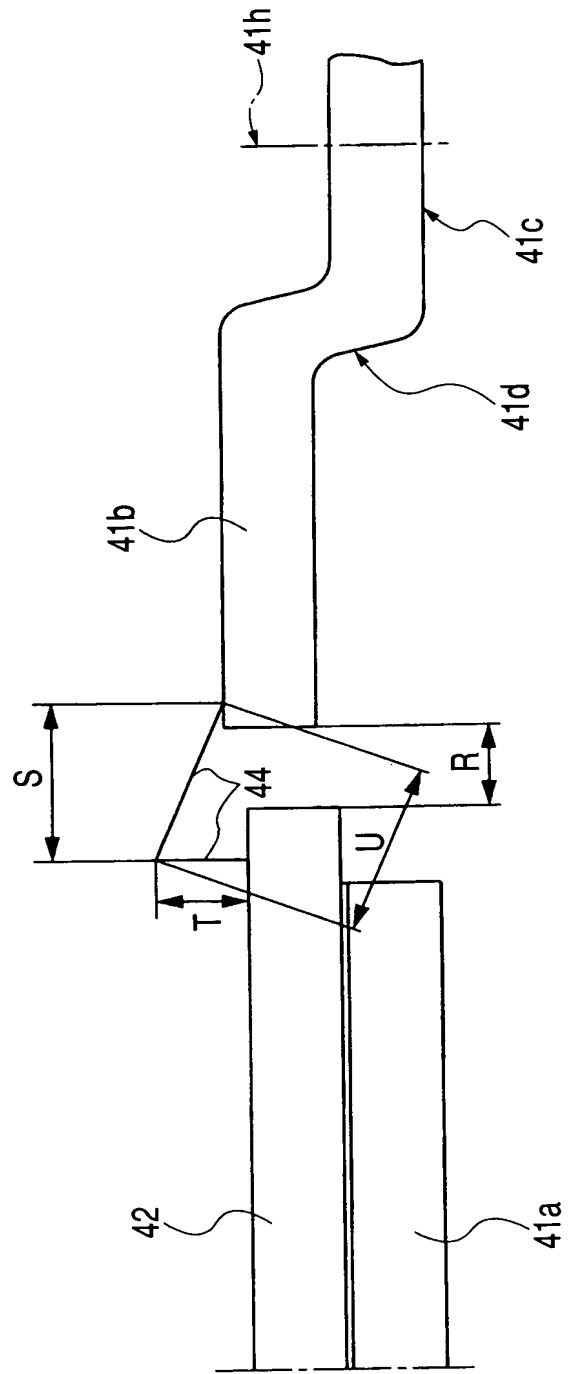
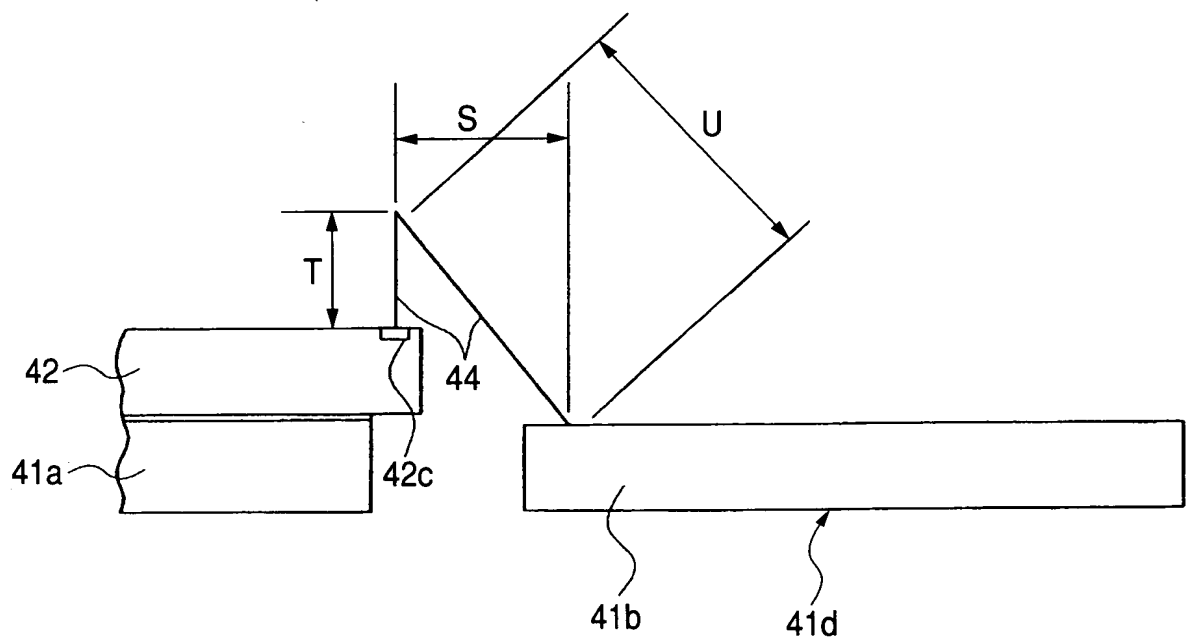
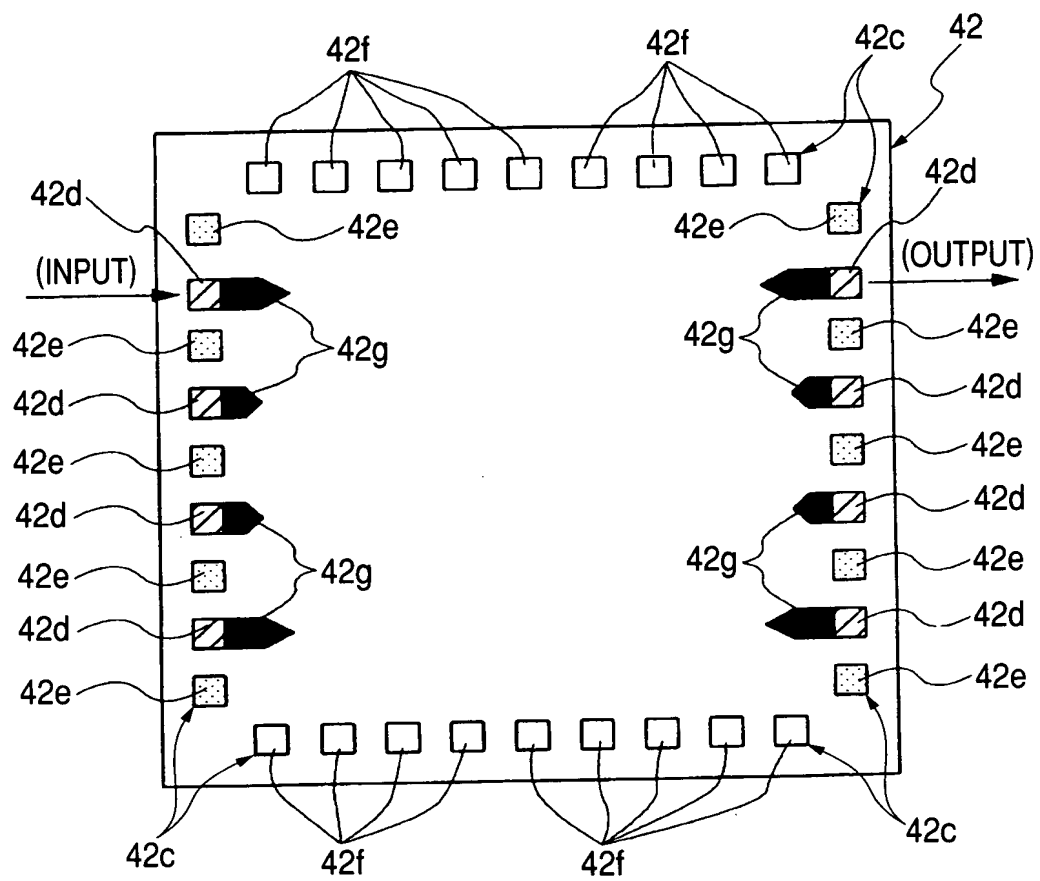


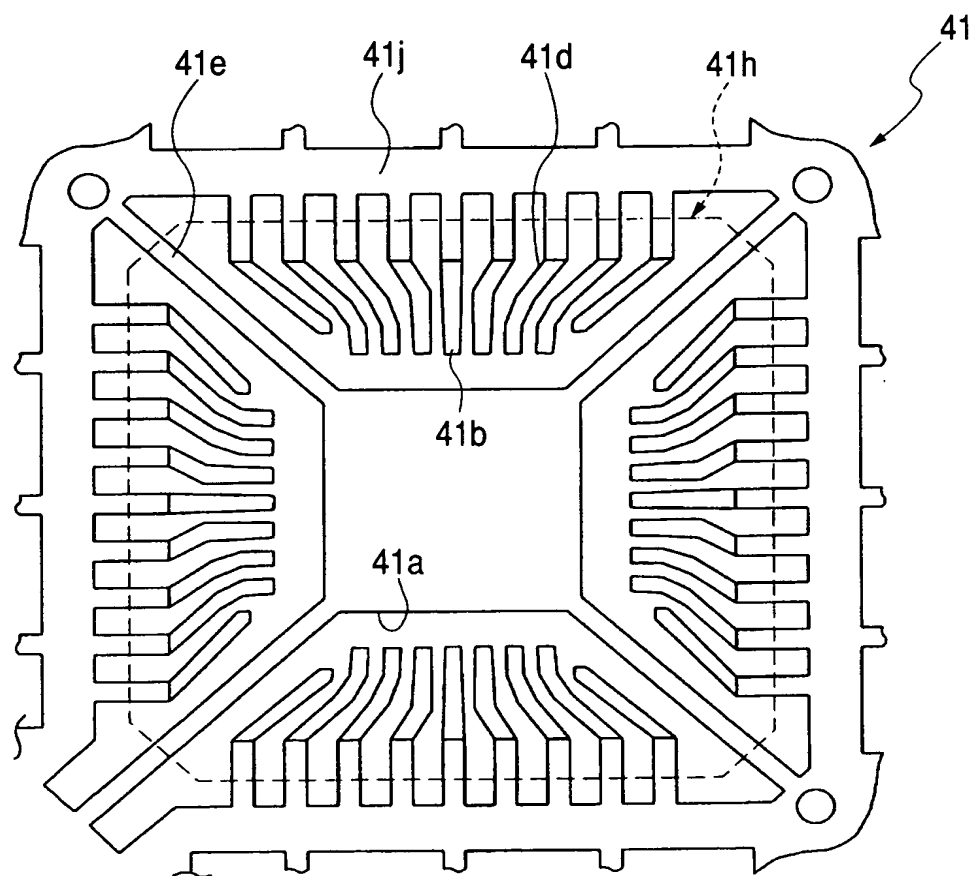
FIG. 21



*FIG. 22*

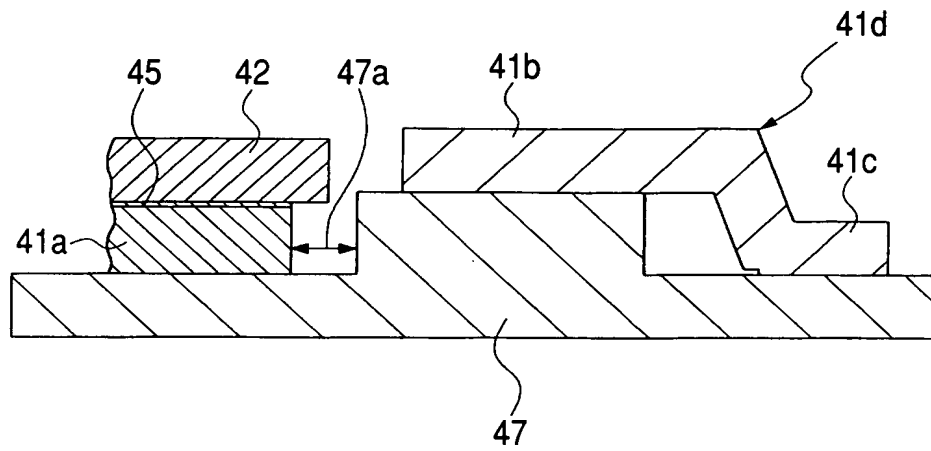
**FIG. 23**

**FIG. 24**

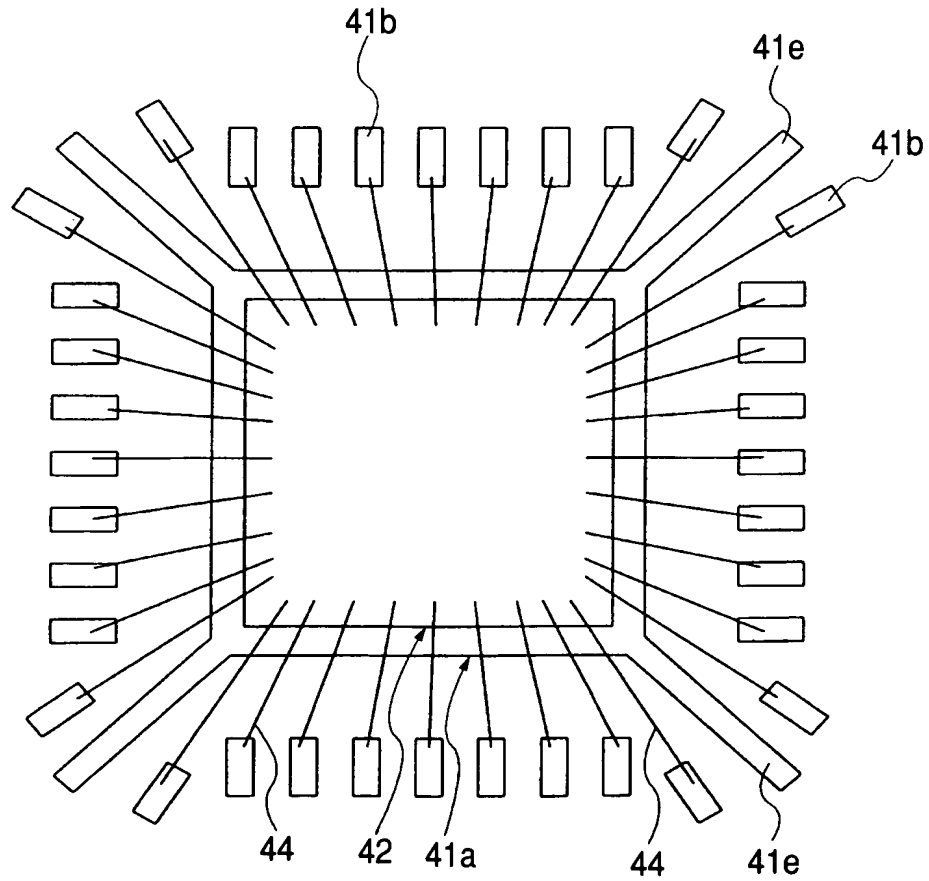


41 : LEAD FRAME

**FIG. 25**

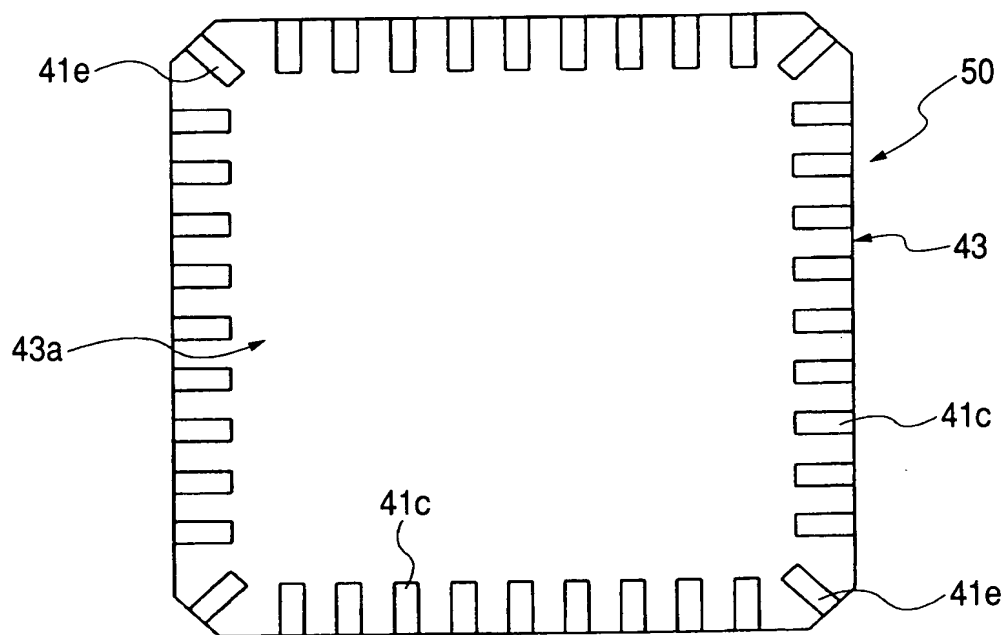


**FIG. 26**

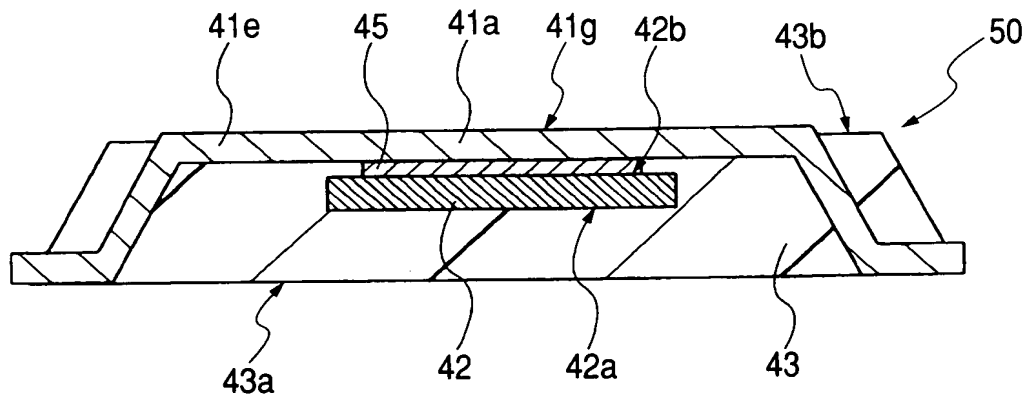




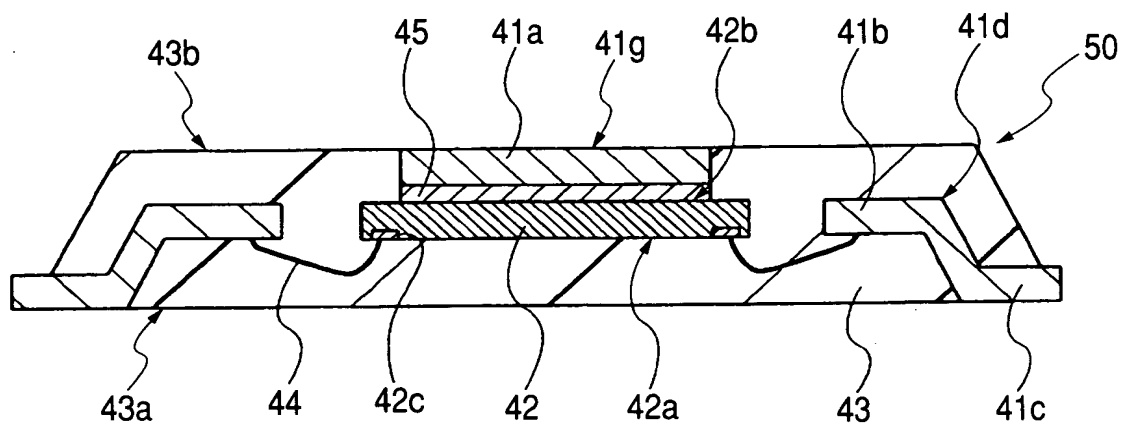
**FIG. 29**



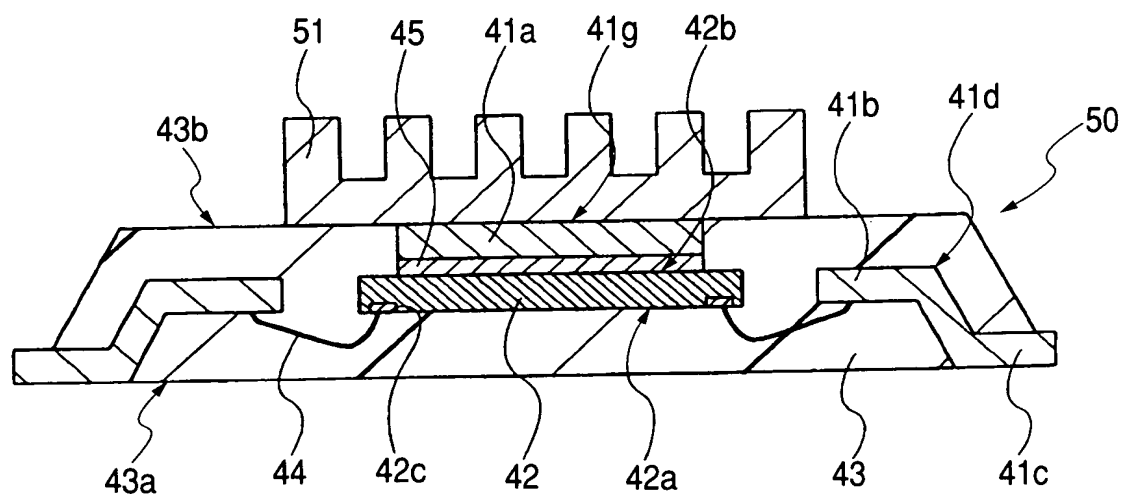
**FIG. 30**



**FIG. 31**

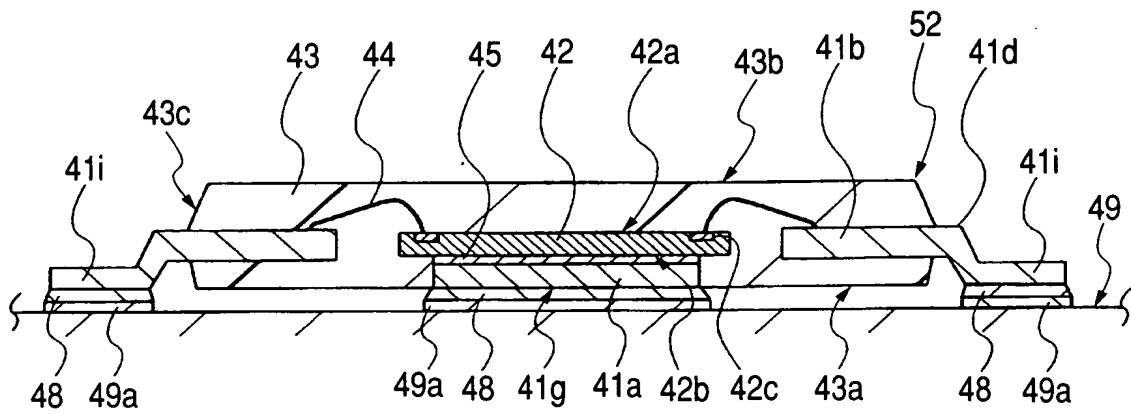


**FIG. 32**



51 : HEAT RADIATION FIN (HEAT SINK)

**FIG. 33**



41i : OUTER LEAD (OUTER TERMINAL PORTTION)

43c : SIDE FACE

52 : QFP (SEMICONDUCTOR DEVICE)